UNITED STATES PATENT APPLICATION

OF

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For

METHOD FOR FABRICATING NONVOLATILE MEMORY DEVICE

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BACKGROUND OF THE INVENTION

Field of the Invention

[01] The present invention relates to a method for fabricating a memory device and, more particularly, to a method fabricating a nonvolatile memory device such as electrically erasable programmable ROM (EEPROM).

Background of the Related Art

[02] With the development of high-capacity memory devices, nonvolatile memory devices are being increasingly important. An example of the nonvolatile memory device is EEPROM.

[03] In the EEPROM, a tunneling region is formed under a floating gate region. Here, the tunneling region has to be narrower than the floating gate region in order to ensure high coupling ratio. The tunneling region is defined as a tunnel window. The tunnel window is one of most important parts in a nonvolatile memory device. The memory device operates by movement of electrons through the tunnel window.

[04] Fig. 1 illustrates, in a cross-sectional view, a structure comprising an oxide pattern 10 and a gate poly pattern 14 on a substrate 10. Here, "L1" indicates a tunnel window. Fig. 2 is a graph illustrating relation between the width of tunnel

window and the coupling ratio in a nonvolatile memory device. The coupling ratio increases as the width of the tunnel window becomes narrower. Therefore, present technology now focuses on the development of the process for forming a narrow tunnel window.

[05] Figs. 3a and 3b illustrate, in cross-sectional views, the fabricating process of a nonvolatile memory device according to a conventional method.

[06] Referring to Fig. 3a, an oxide layer 32 is formed on a substrate 30 and a photoresist pattern 34 is formed on the oxide layer 32. Referring to Fig. 3b, some part of the oxide layer 32 is removed by an etching process using the photoresist pattern 34 as a mask to form an oxide pattern 32a. The etching process is generally wet etching and, therefore, the oxide pattern 32a is etched isotropically. As a result, linewidth of the region etched in the oxide pattern 32a is broader than the linewidth defined by the photoresist pattern. Such broadened linewidth results in low coupling ratio, thereby causing deterioration of device characteristics.

[07] In manufacturing a semiconductor device, a lot of methods for shrinking critical dimension of any structure have been proposed. Among them, U.S. Patent No. 6,579,808, Cho et al., discloses a method for fabricating a semiconductor device capable of maintaining contact hole of fine size when the contact hole for bit line formation is defined. The disclosed method by the

Cho et al. patent comprises forming an insulating layer and an ARC (anti-reflective coating) layer on a substrate; removing some part of the ARC layer through a first dry etching process using a photoresist pattern as a mask and, at the same time, attaching polymers resulting from the dry etching process to the remaining ARC layer to form a polymer sidewall; and removing some part of the insulating layer through a second dry etching process using the photoresist pattern and the polymer sidewall as a mask to form a contact hole.

[08] As another example, U.S. Patent No. 6,368,974, Tsai et al., proposes a method for shrinking equivalent critical dimension of mask by in situ polymer deposition and etching. In the method by Tsai et al. patent, a polymer layer is formed on a photoresist layer and etched by a plasma reactor with at least two independent power sources. Here, voltages of all power source are adjusted such that etching rate and depositing rate are equivalent on surface of the photoresist layer and etching rate is larger than depositing rate in bottom of any structure of the photoresist layer. Therefore, the sidewall of any structure is filled by a conformal polymer layer and, then, width of any structure is efficiently decreased. Accordingly, the critical dimension of any structure is significantly smaller than critical dimension of the mask.

[09] As another example, U.S. Patent 6,319,822, Chen et al., discloses a method for etching of sub-quarter micron openings in insulating layers for contacts and via. The method by Chen et al. patent uses a hardmask formed of carbon enriched titanium nitride. The carbon is released as the hardmask erodes during plasma etching and participates in the formation of a protective polymer coating along sidewalls of the opening etched in the insulating layer. The protective sidewall polymer inhibits lateral chemical etching.

SUMMARY OF THE INVENTION

[10] Accordingly, the present invention is directed to a method of fabricating a nonvolatile memory device that substantially obviates one or more problems due to limitations and disadvantages of the related art.

[11] An object of the present invention is to provide a method for forming an oxide pattern, which defines tunnel window size, so that the tunnel window can have the same linewidth with that defined originally in fabricating a nonvolatile memory device.

[12] Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be

learned from practice of the invention. The objectives and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[13] To achieve these objects and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the present invention provides a method for fabricating a nonvolatile memory device comprising the steps of:

forming a lower insulating layer and a sacrificial layer in sequence on a substrate;

forming a sacrificial layer pattern by removing some part of the sacrificial layer through an etching process to expose some part of the lower insulating layer, wherein spacers are formed on sidewalls of the sacrificial layer pattern, the spacers being formed of polymers resulting from the etching of the sacrificial layer;

removing the exposed lower insulating layer to form a lower insulating layer pattern; and

removing the sacrificial layer pattern and the spacers.

[14] Subsequently, an upper oxide layer with uniform thickness is formed on the lower insulating layer pattern and a gate poly is formed on the upper oxide layer. As a result, a gate

electrode of a nonvolatile memory device such as EEPROM is completed.

[15] Here, the lower insulating layer is preferably formed of oxide and the sacrificial layer is preferably formed of nitride. The spacers preferably have a width between 300Å and 1000Å.

[16] The present invention uses the spacers resulting from etching of the sacrificial layer as an etching mask and, therefore, the region etched in the lower insulating layer pattern can have narrow linewidth. Therefore, linewidth of the tunnel window, which is defined by the linewidth of the region etched in the lower insulating layer pattern, becomes narrow. By reducing the linewidth of the tunnel window, the present invention can ensure high coupling ratio, thereby improving device characteristics.

[17] It is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[18] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application,

illustrate embodiment(s) of the invention and together with the description serve to explain the principle of the invention. In the drawings;

[19] Fig. 1 illustrates, in a cross-sectional view, a structure comprising an oxide pattern and a gate poly pattern;

[20] Fig. 2 is a graph illustrating relation between width of a tunnel window and coupling ratio in a nonvolatile memory device;

[21] Figs. 3a and 3b illustrate, in cross-sectional views, the fabricating process of a nonvolatile memory device according to a conventional method; and

[22] Figs. 4a through 4f illustrate, in cross-sectional views, the fabricating process of a nonvolatile memory device according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[23] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

[24] Referring to Fig. 4a, a lower insulating layer 42 and a sacrificial layer 44 are formed in sequence on a substrate 40. Here, the lower insulating layer 42 is preferably formed of oxide. The sacrificial layer 44 is preferably formed of nitride because a lot of polymers have to be generated while the sacrificial

layer 44 is etched and because the lower insulating layer 42 is formed under the sacrificial layer 44.

[25] Referring to Figs. 4b and 4c, a photoresist pattern (not shown) is formed on the sacrificial layer 44. Then, an etching process is performed using the photoresist pattern as a mask to form a sacrificial layer pattern 44a. Here, the photoresist pattern can be sufficiently formed by using a source of light with a wavelength of i-line because spacers are formed as described in the following. In this regard, the present invention can reduce manufacturing costs by using the wavelength of i-line that is relatively easily applicable.

[26] During the etching process, polymers are generated from the etching. The polymers are attached to sidewalls of the sacrificial layer pattern 44a etched to form spacers 44b. The spacers 44b preferably have a width between 300Å and 1000Å. As a result, the etched region of the sacrificial layer pattern 44a has narrower linewidth than that defined by the photoresist pattern because of the spacers 44b.

[27] Referring to Fig. 4d, an etching process is performed by using the photoresist pattern (not shown) and the sacrificial layer pattern 44a including the spacers 44b as an etching mask to form a lower insulating layer pattern 42a. The etching process is wet etching and, therefore, the lower insulating layer pattern 42a is etched isotropically. However, the linewidth of the region

etched in the lower insulating layer pattern 42a does not become broader than the linewidth defined by the photoresist pattern although the isotropic etching is performed, because the sacrificial layer pattern 44a including the spacers 44b is used as an etching mask. Thus, the region etched in the lower insulating layer pattern 42a can have the desired linewidth and, therefore, the tunnel window defined by the lower insulating layer pattern 42a can maintain the desired linewidth.

[28] Referring to Fig. 4e, the photoresist pattern, the sacrificial layer pattern 44a, and the spacers 44b are removed. Referring to Fig. 4f, an upper oxide pattern is formed on the lower insulating layer pattern 42a to form an oxide pattern 50, a tunnel oxide. Then, a gate poly is formed on the oxide pattern 50 to complete a gate electrode structure of EEPROM.

[29] The present invention uses a sacrificial layer pattern having spacers as an etching mask and, therefore, can easily adjust linewidth of region etched in an oxide pattern which defines a tunnel window. Thus, the present invention can improve device characteristics by increasing coupling ratio. In addition, if deep UV-line is used as a source of light and a dry etching process is performed in manufacturing a nonvolatile memory device, it may increases manufacturing costs although it can easily adjust the linewidth of region etched in the oxide pattern. However, the present invention can reduce manufacturing costs by

employing i-line as a source of light and performing wet etching. Therefore, the present invention can improve productivity and reliability in manufacturing a nonvolatile memory device.

[30] The foregoing embodiments are merely exemplary and are not to be construed as limiting the present invention. The present teachings can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art.